Total No. of Questions : 8] [Total No. of Printed Pages : 3

Paper Code : 23361

EC-403 (T)

B.Tech. IVth Year (Seventh Semester) Examination-2021

(New Syllabus)

(EC Engg. Branch)

VLSI DESIGN AND CIRCUITS

Time : Three Hours] *[Maximum Marks : 70*

Note : Attempt any **five** questions. **All** questions carry equal marks.

1. (a) Explain how inversion is created in MOS structures. Explain the threshold voltage with and without body of a MOS device and explain its significance. 7

   (b) Explain and draw output characteristics of Gradual channel approximation and the channel length modulation in MOSFET. 7

2. (a) Draw a stick diagram for 2 input NAND logic gate using CMOS logic. 7

   (b) Derive the expression for V_{IH}, V_{IC}, N_{ML} and N_{MH} for CMOS inverter. 7

3. (a) Derive the expression for total power dissipation of a CMOS circuit. 7

   (b) Explain the working of pass transistor circuit. 7

4. (a) Design a 4×1 multiplexer using Transmission Gate (TG). 7

   (b) Explain read/write operation of SRAM memory cell. 7

5. (a) Implement the Boolean function Y=AB+(C+D)(E+F)+GH using Domino CMOS logic. 7

   (b) Draw stick diagrams for super buffers and explain them. 7

6. (a) What do you mean by intercorrect? How to estimate interconnect parasities? 7

(b) What is the stick diagram? Draw the stick diagram of 2-input CMOS NOR gate. 7

7. (a) Write short note on DRAM cell. 7

(b) Explain decode and selector circuit. 7

8. Write short notes on any **four** of the following: 3½×4=14

(i) Ratio Logic Model

(ii) Resistive noise coupling

(iii) Clock CMOS logic Evaluate

(iv) Dynamic MOS storage circuit

(v) EEPROM

(vi) Optimum precharge voltage concept