

Total No. of Questions : 7] [Total No. of Printed Pages : 3

**Paper Code : 21325**

**F-425**

**B.C.A. (Vth Semester)  
Examination, 2019-20**

**(New Course)**

**ADVANCED COMPUTER ARCHITECTURE**

**Paper-BCA-505-N**

**Time : 3 Hours ]**

**[ Maximum Marks : 70**

**Note :-** Attempt any *five* questions. All questions carry equal marks. Symbols used have their usual meanings.

1. (a) What are the limitations of instruction-level parallelism ? Explain briefly.
- (b) Explain the four machine organizations according to Flynn's classification.
- (c) Briefly explain the alternative flow control strategies in any message passing system. 4,4,6
2. (a) What are different addressing techniques of cache memory ? Explain with example.

**SE-208**

**( 1 )**

**Turn Over**

- (b) How cache memory and virtual memory are different from main memory of the processor ? Explain the significance of each memory type. 8,6

3. (a) Differentiate between linear pipeline and non-linear pipeline processor.
- (b) Distinguish between arithmetic and logical shifts. Show that in the former case signs are preserved.
- (c) Vectorizing compilers generally defect loops that can be executed on a pipelined vector computer. Are the vectorization algorithms used by vectorizing compilers suitable for MIMD machine parallelization ? Justify your answer. 4,4,6
4. (a) What are SIMD array processors ? Explain with suitable example and figure how communication takes place among the processing elements. <http://www.mjpruonline.com>
- (b) Explain hypercube processor organization. 9,5
5. (a) Differentiate between Loosely Coupled System (LCS) and Tightly Coupled System (TCS) and state which of the coupling systems is better for higher degree of interactions between tasks.

**SE-208**

**( 2 )**

- (b) Explain the difference among the UMA, NUMA and COMA computer memory organisation models.
- (c) Explain the crossbar switch interconnection network. 4,6,4
6. (a) Explain briefly how RISC architecture attempts to reduce execution time.
- (b) What is VLIW (Very Large Instruction Word) and how is it different from RISC or CISC ?
- (c) Suggest how VLIW architecture can achieve superscalar performance. 4,4,6
7. Write short notes on the following :
- (a) Speedup, latency and Throughput
- (b) Moore's law
- (c) Iron law of processor performance
- (d) Amdahl's law for vectorization 3,3,3,5

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( 3 )